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IN THE SPECIFICATION:

Please amend paragraph [0028] as follows:

[0028] The invention includes methods for fabricating a via through the thickness of a wafer or other substrate, wherein the via includes a conductive liner material and a filler material. The filler material may be a conductive or nonconductive material. Referring now to drawing FIG. 5A, there is shown a cross-section of a semiconductor component generally at 100. The semiconductor component 100 includes a substrate 112 having a first surface 114 and an ~~opposing~~ opposing, second surface 116. The substrate 112 may comprise an unprocessed semiconductor wafer or other substrate, wherein the substrate may have various process layers formed thereon including one on more semiconductor layers or other structures. The substrate 112 may further include active portions or other operable portions located thereon fabricated by etching, deposition or other known techniques. The substrate 112 may further comprise an interposer substrate for use between a test device and a semiconductor device to be tested (contactor board) or between a memory device and system in a package to provide routing among other substrates. In the exemplary embodiment, the substrate 112 comprises a semiconductor ~~material~~ material, such as monocrystalline silicon. In other embodiments, the substrate 112 may comprise polycrystalline silicon, germanium, silicon-on-glass, silicon-on-sapphire, a ceramic, a polymer or a glass-filled, epoxy resin material. The substrate 112 may also comprise any other known substrate material.

Please amend paragraph [0040] as follows:

[0040] Since the seed layer 128 extends to a plane or level even with the first surface 114 and the second surface 116 of the substrate 112, the deposition of the conductive layer 130 may result in a small portion 132 of the conductive layer 130 extending beyond the plane of the first surface 114 or the second surface 116 of the substrate 112. The small portion 132 may be removed, if desired, using CMP or other known removal ~~process~~ processes such that the conductive layer 130 is substantially even with the plane of the first surface 114 and the second surface 116 of the substrate 112 as illustrated in drawing FIG. 5E.

Please amend paragraph [0044] as follows:

[0044] In another exemplary embodiment, a blind via may be used to form the conductive via of the present invention. A cross-section of a semiconductor component is shown generally at 200 in FIG. 6A. The semiconductor component 200 comprises a substrate 212 having a first surface 214 and an ~~opposing~~ opposing, second surface 216. The substrate 212 may comprise an unprocessed semiconductor wafer or other substrate material used in fabrication processes as previously described herein with reference to the substrate 112 of FIG. 5A.